

Please amend the specification as follows:

[0027] Referring now to **FIGURE 4**, there is illustrated a block diagram of an exemplary decoder 400 in accordance with an embodiment of the present invention. A processor, that may include a CPU 490, reads an MPEG transport stream 428 into a transport stream buffer 432 within an SDRAM 430. The data is output from the transport stream presentation buffer 432 and is then passed to a data transport processor 435. The data transport processor then demultiplexes the MPEG transport stream into its PES constituents and passes the audio transport stream to an audio decoder 460 and the video transport stream to a video transport processor 440. The video transport processor 440 converts the video transport stream into a video elementary stream and provides the video elementary stream to an MPEG video decoder 445 that decodes the video. The audio data is sent to the output blocks and the video is sent to a display engine 450. The display engine 450 is responsible for and operable to scale the video picture, render the graphics, and construct the complete display, among other functions. Once the display is ready to be presented, it is passed to a video encoder 455 where it is converted to analog video using an internal digital to analog converter (DAC). The digital audio is converted to analog in the audio digital to analog converter (DAC) 465, or SPDIF generator 470.